REMARKS

Claims 1-10 are pending in the present application. Claims 9 and 10 have been added, and claims 4, 7, and 8 have been amended herein. No new matter has been added.

The drawings have been objected to because they do not have the "required bubbles." Applicant respectfully submits that the drawings, as filed, clearly and accurately depict the illustrated embodiment. That being said, to move matters along, replacement sheet drawings have been attached herewith and include bubbles as requested by the Examiner.

Claims 4-7 have been rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention. The preamble of claim 4 has been amended to recite an apparatus, which is clearly descriptive of the claimed invention. Claims 7 and 8 have been likewise amended. Applicant notes that claims 5 and 6 are related to a method and, therefore, this rejection does not apply.

Claim 1 has been rejected under 35 U.S.C. § 102(b) as being anticipated by Winebarger. Applicant respectfully submits that claim 1, as originally filed, is allowable over the references of record.

Claim 1, as originally filed, specifically requires that the reset signal is "for resetting a microprocessor." Winebarger, on the other hand, makes no mention of microprocessors and, therefore, cannot teach or suggest a "reset signal for resetting a microprocessor." Since the reference does not teach each and every element of the claimed invention, it cannot anticipate the claim.

Claim 1 further requires "a comparator for generating a shortfall signal indicative of a shortfall of the supply voltage in relation to a reference voltage." This element is not taught or

suggested by the Winebarger reference. Claim 1 further recites that "the outputs of the integrator is used to generate a reset signal for resetting a microprocessor." This element is not taught or suggested by the Winebarger reference.

The Office Action is incorrect to assert that Winebarger discloses using an integrator to integrate the output of the comparator. The resistor-capacitor (R-C) combination 68, 70 of Figure 2 of Winebarger is not set up as an integrator. An integrator circuit would require at least the input of the resistor in the R-C combination to be supplied from the output of the comparator and the output of the resistor to be connected to the positive terminal of the capacitor. It is therefore clear that the R-C combination of Winebarger does not provide an integrator circuit and, therefore, does not provide an integration function.

The R-C combination 68, 70 of Winebarger actually acts as an analog delay with a time constant (defined by the product of the values of R4 and C2) to keep the POR output active (HIGH) after the supply voltage +V has increased beyond a certain threshold and the output of the comparator changes state from LOW to HIGH (the output on line 61 of the comparator 46 is inverted by inverter 60 to produce the POR signal). For a discussion of this, refer to col. 4, lines 38-52 of Winebarger.

The R-C delay function is only active when the output 61 of comparator 46 switches to HIGH; i.e., in the transient state from LOW to HIGH. The time constant of the combination R4, C2 is such that the voltage on line 61 will build up at a rate according to the time-constant of R4, C2, thereby delaying the point by which the inverter 60 output changes state to go LOW, to remove the POR signal (see Fig. 3 and col. 5, line 12 to line 37 of Winebarger).

Thus it is clear that the output of the comparator in Winebarger is not integrated, but merely subjected to a time delay in the transient state of the comparator output going HIGH. It is

therefore a logical consequence of this that Winebarger does not disclose that the output of the integrator is used to generate a reset signal either.

In contrast to this, the present invention provides for the time-integration of the output of the comparator, regardless of the value of the output of the comparator, to provide a reset signal. Claim 1 is therefore clearly novel over Winebarger.

Claims 2-3 depend from claim 1 and add further limitations. It is respectfully submitted that these claims are allowable because they depend from an allowable claim as well as add further limitations.

Claims 4-6 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over Winebarger. Applicant respectfully traverses this rejection.

Claim 4, as originally filed, recites "an under voltage detection (UVD) circuit that includes a comparator for generating a shortfall signal indicative of a shortfall of the supply voltage in relation to a reference voltage, and an integrator for time-integrating the shortfall signal to form an integrated signal, wherein the output of the integrator is used to generate a reset signal for resetting the microprocessor, and reset means arranged to receive the reset signal output by the UVD circuit and according to its value to initiate a reset of the microprocessor [circuitry]." The references of record do not teach or suggest the limitations of claim 4.

The distinctions of the claimed invention over Winebarger discussed above with respect to claim 1 also apply to claim 4. Further, a person skilled in the art, seeking to arrive at the present invention, has no motivation to consult with Winebarger. Even if the skilled person did consult with Winebarger, he would find no teaching in Winebarger to point him to the invention of claim 4.

In the present invention, the output of the comparator, the "shortfall signal," is time-integrated. An advantage of this is that the comparator can produce an output current that varies with the voltage difference at its inputs (page 3, lines 19-23 of the present application as filed, PCT publication). This "difference" current is then integrated with respect to time, the advantage arising from the fact that both the magnitude of the comparator input voltage difference and its time duration are considered in generating the reset signal. Further, the integration of the comparator output is active irrespective of the value of the comparator output and whether the output is going HIGH or LOW.

This is in stark contrast to the Winebarger circuit. The comparator of Winebarger acts as a digital switch, switching between HIGH (no undervoltage condition) and LOW (undervoltage condition). Thus, the "shortfall signal" generated by Winebarger is a LOW (or zero) signal. There is no point whatsoever in time-integrating this zero "shortfall signal" as the result would of course also be zero and, therefore, of no practical use. Thus, Winebarger positively teaches away from the present invention; the present invention must be considered non-obvious in light of this document.

The integration of this shortfall signal means that the magnitude of the comparator input voltage difference is taken into account in the present invention. Circuits according to the present invention are therefore able to differentiate between small, medium and large input voltage difference magnitudes. This is another technical advantage the present invention provides over Winebarger, which cannot operate in this fashion.

Furthermore, replacement of the R-C combination of Winebarger with an integrator would mean that the circuit of Winebarger simply would not work as required. One reason for

this is that the potential of line 61 could not be tied by resistor R4, 68 to terminal 12, a requirement of the Winebarger circuit (col. 4, lines 41, 42).

Simply put, there is no reasonable or logical adaptation of Winebarger by which the person skilled in the art could arrive at the present invention. Claim 4 is therefore non-obvious over Winebarger.

Claims 1-2 and 4-7 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Yoshimura in view of Woods. Applicant respectfully traverses this rejection.

Applicant respectfully submits that the rationale of the Office Action is based upon erroneous conclusions. It is not obvious to the person skilled in the art to replace the delay circuit of Yoshimura with the R-C delay circuit of Woods. This is because the delay circuit of Yoshimura is a delay circuit in a digital logic circuit, while the delay circuit in Woods is a delay circuit in an analog circuit for monitoring undervoltages in a digital power supply. Thus, the skilled person simply would not combine the Yoshimura and Woods documents as they provide entirely incompatible teachings.

A typical digital delay circuit provides a means for delaying the entire signal waveform; that is, the signal is effectively time-shifted by the digital delay circuit. (As evidence that this is a requirement of the digital delay circuit 7 in Yoshimura, refer to column 4, line 60 *et seq.* and Figure 5.) On the other hand, in a typical R-C analogue delay circuit, the effect of the circuit is that the rate at which the output voltage level rises to a peak is delayed; the circuit does not time-shift the entire waveform shape as in a digital delay circuit. Woods does discuss at, for example, col. 2, lines 40 to 50 that "delay circuit 130 that provides an output, voltage V_b, that is slightly delayed from its input transitions in voltage V_d". However, the person skilled in the art would

take from this teaching that the delay being discussed is a delay in the rate of rise of the output voltage of the delay circuit and not a time-shift delay as provided in a digital delay circuit.

As such, the analogue delay circuit of Woods simply has no place in a digital logic circuit and would be unable to re-produce the effect desired by the digital delay circuit of Yoshimura. The exponential charging/discharge property of the R-C circuit of Woods would not provide the time-shift effect of the digital delay element of Yoshimura and is incapable of producing the Vb/Vc waveforms of Figures 5, 6 and 7 of Yoshimura.

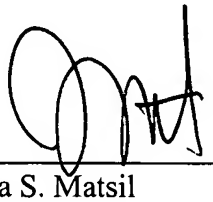
A logical consequence of this is that the skilled person would not combine Yoshimura and Woods and claim 1 is non-obvious over this combination of documents.

Thus, claim 1 is novel and non-obvious over all the prior art documents. Similar comments apply also to claims 4 and 5 which, therefore, are also patentable. The dependent claims, by virtue of their dependencies at least, are also non-obvious.

Claims 9 and 10 are added herein. Claim 9 is a rewritten version of claim 3 and claim 10 is a rewritten version of claim 8 (where the term "microprocessor" has been replaced with the term "apparatus"). The Office Action has indicated that these claims are allowable.

In view of the above, Applicant respectfully submits that the application is in condition for allowance and requests that the Examiner pass the case to issuance. If the Examiner should have any questions, Applicant requests that the Examiner contact Applicant's attorney at the address below. In the event that the enclosed fees are insufficient, please charge any additional fees required to keep this application pending, or credit any overpayment, to Deposit Account No. 50-1065.

Respectfully submitted,



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